What is claimed is:

1. A substrate comprising:

a conductive plane;

a via passing through the conductive plane;

wherein the conductive plane contacts the via to electrically interconnect the via and the conductive plane; and

wherein a gap separates a surface of the via from the conductive plane to provide an uninterrupted path for electrical current flowing substantially on the surface of the via.

2. The substrate of claim 1, wherein the via is adapted to interconnect an electronic component disposable on one side of the substrate and an electronic component disposable on an opposite side of the substrate.

3. The substrate of claim 1, wherein a tab lying substantially in a plane of the conductive plane contacts the via.

4. The substrate of claim 1, wherein two or more tabs lying substantially in a plane of the conductive plane contact the via.

5. The substrate of claim 1, wherein the conductive plane comprises two or more conductive planes and wherein the gap comprises two or more gaps that respectively separate the two or more conductive planes from the via.

6. The substrate of claim 5, wherein a portion of each of the two or more gaps is aligned with a portion of another of each of the two or more gaps.

7. A substrate comprising:

a conductive plane;

a via passing through the conductive plane;

wherein a gap separates a surface of the via from the conductive plane to provide an uninterrupted path for electrical current flowing substantially on the surface of the via; and

wherein a tab of the conductive plane spans the gap and contacts the via to electrically interconnect the via and the conductive plane.

8. The substrate of claim 7, wherein the via is adapted to interconnect an electronic component disposable on one side of the substrate and an electronic component disposable on an opposite side of the substrate.

9. The substrate of claim 7, wherein the tab comprises two or more tabs.

10. The substrate of claim 7, wherein the conductive plane comprises two or more conductive planes and wherein the gap comprises two or more gaps that respectively separate the two or more conductive planes from the via.

11. The substrate of claim 10, wherein a portion of each of the two or more gaps is aligned with a portion of another of each of the two or more gaps.

12. A substrate comprising:

first and second conductive planes substantially parallel to each other;

first and second vias respectively passing through the first and second conductive planes, wherein the first and second vias are adapted to interconnect a first electronic component disposable on a first side of the substrate and a second electronic component disposable on a second side of the substrate;

wherein the first conductive plane contacts the first via to electrically interconnect the first via and the first conductive plane and the second conductive plane contacts the second via to electrically interconnect the second via and the second conductive plane; and

wherein a first gap separates a surface of the first via from the first conductive plane to provide an uninterrupted path for electrical current flowing substantially on the surface of the first via and wherein a second gap separates a surface of the second via from the second conductive plane to provide an uninterrupted path for electrical current flowing substantially on the surface of the second via.

13. The substrate of claim 12, wherein a tab lying substantially in a plane of the first conductive plane contacts the first via.

14. The substrate of claim 13, wherein the tab spans the first gap.

15. The substrate of claim 13, wherein the tab comprises two or more tabs.

16. The substrate of claim 12, wherein a tab lying substantially in a plane of the second conductive plane contacts the second via.

17. The substrate of claim 16, wherein the tab spans the second gap.

18. The substrate of claim 16, wherein the tab comprises two or more tabs.

19. The substrate of claim 12, wherein the first conductive plane comprises two or more first conductive planes and wherein the first gap comprises two or more first gaps that respectively separate the two or more first conductive planes from the via.

20. The substrate of claim 19, wherein a portion of each of the two or more first gaps is aligned with a portion of another of each of the two or more first gaps.

21. The substrate of claim 12, wherein the second conductive plane comprises two or more second conductive planes and wherein the second gap comprises two or more second gaps that respectively separate the two or more second conductive planes from the via.

22. The substrate of claim 21, wherein a portion of each of the two or more second gaps is aligned with a portion of another of each of the two or more second gaps.

23. A method for transmitting high-frequency current through a substrate, the method comprising:

receiving the high-frequency current at a via passing through a conductive plane disposed within a substrate; and

directing the high-frequency current along an uninterrupted path substantially on a surface of the via comprising:

separating the via from the conductive plane using a gap, and

spanning the gap with one or more tabs of the conductive plane so that the one or more tabs contact the via.

24. The method of claim 23, wherein receiving the current at the via comprises receiving the current from an electronic component disposed on the substrate.

25. The method of claim 23, wherein receiving the high-frequency current at a via passing through a conductive plane disposed within a substrate comprises receiving the high-frequency current at a via passing through two or more conductive planes disposed within the substrate.

26. The method of claim 25, wherein directing the high-frequency current along an uninterrupted path substantially on the surface of the via comprises:

separating the via from each of the two or more conductive planes respectively using each of two or more gaps;

aligning a portion of each of the two or more gaps with a portion of another of each of the two or more gaps; and

respectively spanning each of the two or more gaps with one or more tabs of each of the two or more conductive planes so that the one or more tabs of each of the two or more conductive planes contact the via.

27. A method for connecting a via to a conducting plane, the method comprising:

passing the via through an aperture in the conducting plane such that a gap exists between a surface of the via and the conducting plane, wherein the gap provides an uninterrupted path for electrical current flowing substantially on the surface of the via; and

spanning the gap with a tab of the conducting plane so that the tab contacts the via.

28. The method of claim 27, wherein spanning the gap with a tab comprises spanning the gap with two or more tabs.

29. A method for manufacturing an electronic circuit board, the method comprising:

forming a conductive plane within a substrate;

forming a via within the substrate that passes through the conductive plane and makes contact with the conductive plane; and

forming a gap between a surface of the via and the conductive plane, wherein the gap provides an uninterrupted path for current flowing substantially on the surface of the via.

30. The method of claim 29, wherein forming a gap between a surface of the via and the conductive plane comprises forming a tab that spans the gap and contacts the surface of the via.

31. The method of claim 30, wherein forming a tab that spans the gap and contacts the surface of the via comprises forming two or more tabs that span the gap and contact the surface of the via.

32. The method of claim 29, wherein forming a conductive plane within a substrate comprises forming two or more conductive planes within the substrate.

33. The method of claim 32, wherein forming a via within the substrate comprises forming two or more vias within the substrate respectively passing through

each of the two or more conductive planes and respectively making contact with each of the two or more conductive planes.

34. A method for manufacturing an electronic circuit board, the method comprising:

forming two or more conductive planes within a substrate;

forming a via within the substrate that passes through each of the two or more conductive planes and makes contact with each of the two or more conductive planes;

forming each of two or more gaps respectively between each of the two or more conductive planes and a surface of the via; and

aligning a portion of each of the two or more gaps with a portion of another of each of the two or more gaps to provide an uninterrupted path for current flowing substantially on the surface of the via.

35. The method of claim 34, wherein forming each of two or more gaps respectively between each of the two or more conductive planes and a surface of the via comprises forming a tab spans each of the two or more gaps and contacts the surface of the via.

36. The method of claim 35, wherein forming a tab that spans each of two or more gaps and contacts the surface of the via comprises forming two or more tabs that span the gap and contact the surface of the via.